Remarks

Figure 9 has had the legend "Prior Art" attached per the Examiner's request.

Claims 1 and 4 have been amended. No new matter has been added. These amendments are based on Fig. 3, which shows an arrangement of the power supply capacitor cells with respect to the logic gates. This Figure shows that the power supply capacitor cells may be connected between a power supply (Vdd) of the logic gate cells and a ground (Vss). The amended claims require that the power supply capacitor cells are connected with a power supply of the logic cells and a ground.

Claims 1-4 have been rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,204,694 to Sunter et al. ("the '694 patent"). Applicants respectfully traverse this rejection.

The capacitors of the cited reference are capacitors for signals (or for frequencies), but not for a power supply as described in the present invention. Thus, this reference is different from the present invention in the functions of these capacitors and does not teach the methods which provide the advantages of the present invention. Also, because the power supply capacitor cells of the present invention are provided for connecting the power supply line of the logic gate and the ground line of the logic gate, it is effective in stabilizing the power supply of the logic gate and reducing the power supply noise. The cited reference provides no such advantage. In the present invention, the logic gate cells operate stably with power supplied from the power supply capacitor cells. This provides the advantage of the present invention: that power supply noise of the entire LSI circuit can be reduced.

Moreover, claim 1 requires determining a capacitance value of the power supply capacitor cells so as to correspond to a drive load capacitor value of the logic gate, which the cited reference does not describe or suggest. The step for determining the capacitance value is also different between the present invention and the reference. The invention of claim 1 can reduce noise for each logic gate. Therefore, the present invention can reduce noise more effectively than in the cited reference, which merely refers to controlling at least two inverters.

Regarding claim 4, the cited reference does not teach or suggest the use of spaces where standard cells are not arranged. Thus, the effect of reducing noise without increasing block area is not obvious from the description of the reference. Moreover, the present invention provides the advantage of arranging the power supply capacitor cells in spaces of each block where standard cells are not arranged by automatic arrangement wiring. The cited reference does not so teach. Thus, the present invention provides an advantage over the cited reference in allowing the reduction of power supply noise without increasing each block area of the LSI.

Finally, the cited reference provides ring oscillators in which a capacitor is arranged at the output side in order to take the output frequency constantly from the ring oscillators (from which output frequency can be freely selected). That is, when the capacitors are arranged at the output sides of the respective ring oscillators, the output capacitance can be increased, and thus the respective ring oscillators can maintain the output capacitance at a same level so as to enable output of constant frequency. By contrast, the present invention has a capacitor functioning in stabilizing the power supply and in suppressing noise while stabilizing the power supply.

Because the cited reference does not teach all of the elements in claims 1 and 4, nor does it suggest the methods described in these claims, they should be allowed. Because the independent claim upon which claims 2 and 3 depend is now in condition for allowance, these dependent claims also should be allowed.

In view of the above, favorable reconsideration in the form of a Notice of Allowance is requested. The Examiner is invited to telephone the undersigned at (612) 371-5237 if there are any issues that prevent the allowance of this application.

May 24, 2002
Date

Respectfully submitted,

MERCHANT & GOULD P.C.
3200 IDS Center, 80 South Eighth Street
Minneapolis, Minnesota 55402
Telephone: (612) 332-5300

Douglas P. Mueller
Reg. No. 30,300
DPM/TRL

VERSION WITH MARKINGS TO SHOW CHANGES MADE IN THE CLAIMS

Claims 1 and 4 have been amended as follows:

1. (Once Amended) A LSI layout method for a LSI design by automatic arrangement wiring of standard cells, wherein logic gate cells and power supply capacitor cells are provided as the standard cells, comprising the operations of :

[providing power supply capacitor cells as one of the standard cells in addition to logic gate cells provided as standard cells,]

determining a capacitance value of the power supply capacitor cells so as to correspond to a drive load capacity value of the logic gate cells [to which the power supply capacitor cells are to be arranged, and],

connecting the power supply line of the logic gate with the ground line of the logic gate through the power supply capacitor cells, and

arranging the power supply capacitor cells in the vicinity of the logic gate cells.

4. (Once Amended) A LSI layout method for a LSI design by automatic arrangement wiring of standard cells, wherein logic gate cells and power supply capacitor cells are provided as the standard cells, comprising the operations of :

[providing power supply capacitor cells as one of the standard cells, and]

connecting the power supply line of the logic gate with the ground line of the logic gate through the power supply capacitor cells, and

arranging the power supply capacitor cells in spaces of each block where standard cells are not arranged by the automatic arrangement wiring.